IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (Original) A method of operating a master/slave system, said method comprising the steps of:

identifying a master receive data phase value to coordinate the transfer of data from a slave device without phase alignment circuitry to a master device with a universal phase aligner;

transferring data from said slave device to said master device in accordance with said master receive data phase value;

characterizing a master transmit data phase value to coordinate the transfer of data from said master device to said slave device; and

routing data from said master device to said slave device in accordance with said master transmit data phase value.

2. (Original) The method of claim 1 wherein said identifying step includes the steps of:

applying an alignment signal from said slave device to said master device; and

aligning a receive data clock signal with said alignment signal to obtain said master receive data phase value.

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3. (Original) The method of claim 2 wherein said identifying step further includes the steps of:

applying a margin offset to said master receive data phase value; and

storing said master receive data phase value.

4. (Original) The method of claim 1 wherein said transferring step includes the steps of:

adjusting a system clock signal in accordance with said master receive data phase value to obtain a master receive data clock; and

receiving data at said master device in response to said master receive data clock.

5. (Original) The method of claim 1 wherein said characterizing step includes the steps of:

routing request bus data received at said slave device to said master device to form re-routed request bus data; and

aligning a receive data clock signal with said re-routed request bus data to obtain said master transmit data phase value.

6. (Original) The method of claim 5 wherein said characterizing step further includes the steps of:

applying a margin offset to said master transmit data phase value; and

storing said master transmit data phase value.

7. (Original) The method of claim 1 wherein said aligning step includes the steps of:

adjusting a system clock signal in accordance with said master transmit data phase value to obtain a master transmit data clock; and

transmitting data from said master device in response to said master transmit data clock.

8. (Canceled) A method of operating a master/slave system, said method comprising the steps of:

assessing a phase delay required for synchronized communication between a master device with a universal phase aligner and a slave device without phase alignment circuitry; and

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communicating data between said master device and said slave device in accordance with said phase delay.

9. (Previously Presented) A method of operating a master/slave system, said method comprising the steps of:

assessing a phase delay required for synchronized communication between a master device with a universal phase aligner and a slave device without phase alignment circuitry;

assigning, based upon said phase delay, a first data signal edge that said slave device does not process and a second data signal edge that said slave device does process; and

communicating data between said master device and said slave device in accordance with said phase delay.

10. (Previously Presented) The method of claim 9 wherein said assessing step includes the step of assessing a plurality of phase delays required for synchronized communication between said master device and a corresponding plurality of slave devices.

11. (Currently Amended) A method of operating a master/slave system, said method comprising the steps of:

assessing a plurality of phase delays ~~required~~ for synchronized communication between a master device ~~with a universal phase aligner~~ and a ~~plurality of~~ slave devices ~~without phase alignment circuitry~~, <u>wherein each phase delay is associated with a different bus connecting the master device and the slave device</u>;

identifying a ~~selected~~ phase delay from said plurality of phase delays for ~~a selected~~ <u>the</u> slave device ~~of said plurality of slave devices~~; and

communicating data between said master device and said ~~selected~~ slave device ~~of said plurality of slave devices~~ in accordance with said ~~selected~~ phase delay.

12. (Currently Amended) The method of claim 11 further comprising the step of designating ~~a selected slave device of said plurality of slave devices~~ <u>the slave device</u> for communication with said master device.

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13. (Currently Amended) The method of claim 12 wherein said designating step includes the step of applying a control signal to a side band bus linking ~~said plurality of slave devices~~ <u>the master device and the slave device</u>.

14. (Currently Amended) The method of claim 12 wherein said designating step includes the step of applying a control signal to a request bus linking ~~said plurality of slave devices~~ <u>the master device and the slave device</u>.

15. (Currently Amended) A master/slave system, comprising:

~~a plurality of slave devices, each slave device including a clock circuit without phase alignment circuitry a slave device~~ <u>a slave device</u>; and

a master device ~~with a universal phase alignment circuit~~ coupled to the slave device and including an addressable phase value register bank adapted for storing a plurality of phase values for ~~said plurality of slave devices~~ <u>said slave device</u>, said master device utilizing a selected phase value of said plurality of phase values ~~to alter a system clock signal in accordance with said selected phase value so as~~ to establish synchronous communication between

said master device and ~~a selected slave device of said plurality of slave devices~~ the slave device.

16. (Currently Amended) The master/slave system of claim 15 wherein said master device utilizes a first selected phase value ~~to alter said system clock signal~~ to establish a master receive data clock signal to receive data from ~~said selected~~ the slave device.

17. (Currently Amended) The master/slave system of claim 16 wherein said master device utilizes a second selected phase value ~~to alter said system clock signal~~ to establish a master transmit data clock signal to transmit data to ~~said selected~~ the slave device.

18. (Currently Amended) The master/slave system of claim 15 wherein said master device performs a calibration operation in connection with ~~each slave device of said plurality of slave devices~~ the slave device to identify said plurality of phase values.

19. (Original) The master/slave system of claim 18 wherein said master device adds an offset value to each phase value of said plurality of phase values.

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20. (Original) In a system comprising a master and at least one slave, the master and at least one slave coupled to a common bus, an auxiliary channel and a common clock, the method of phase aligning an internal clock in the master device and derived from the common clock to enable communication over the data bus with the at least one slave, the method comprising the steps of:

the master causing the at least one slave device to emit a periodic data signal on the data bus by sending a command to the at least one slave device on the auxiliary channel;

the master receiving and sampling the periodic data signal with the internal clock;

the master making a phase adjustment to the internal clock based on the sampled periodic signal to determine a phase boundary of the periodic data signal;

the master storing the value of the phase adjustment in a storage device of the master; and

the master adjusting the phase of the internal clock by the stored phase adjustment value plus an offset to receive data substantially without error from the at least one slave device.

21. (Currently Amended) A method for calibrating transmission of data from a master device to a ~~first~~ slave device over ~~a data line~~ multiple buses, comprising:

determining ~~a~~ phase offset values corresponding to ~~data transmission from the~~ synchronous communication between the master device ~~to~~ and the ~~first~~ slave device over ~~the data line~~ multiple buses;

storing the phase offset values in an addressable register bank in the master device to produce ~~a~~ stored offset values; and

using the stored offset values in the ~~transmission of data from~~ synchronous communication between the master device ~~to~~ and the ~~first~~ slave device over ~~the data line~~ at least one bus.

22. (Currently Amended) The method of claim 21, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on ~~the~~ at least one stored offset value to produce a phase adjusted clock signal; and

transmitting data over ~~the data line~~ at least one bus based on the phase adjusted clock signal.

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23. (Currently Amended) The method of claim 22, wherein transmitting data over ~~the data line~~ at least one bus further comprises driving the data on the ~~data line~~ bus using an output buffer, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

24. (Currently Amended) The method of claim 21, wherein determining the phase offset value further comprises sending data to the ~~first~~ slave device.

25. (Currently Amended) The method of claim 24, wherein the data is sent to the ~~first~~ slave device over a request ~~line~~ bus.

26. (Currently Amended) The method of claim 24, wherein determining the phase offset value further comprises receiving the data sent to the ~~first~~ slave device, from the ~~first~~ slave device.

27. (Currently Amended) The method of claim 26, wherein determining the phase offset value further comprises comparing the phase of the data received from the ~~first~~ slave device with the phase of a clock signal.

28. (Currently Amended) The method of claim 27, wherein the data is sent to the ~~first~~ slave device over a request ~~line~~ bus, and wherein the data is received from the ~~first~~ slave device over ~~the data line~~ a data bus.

29. (Previously Presented) The method of claim 21, wherein the phase offset value is stored with a plurality of additional phase offset values in the master device.

30. (Previously Presented) The method of claim 21, wherein the phase offset value is adjusted by a margin offset.

31. (Previously Presented) A method for calibrating transmission of data from a master device to a first slave device over a data line and a second slave device over a request line, comprising:

determining a phase offset value corresponding to data transmission from the master device to the first slave device over the data line and a control phase offset value corresponding to control information transmission from the master device to the second slave device over the request line;

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storing the phase offset value and the control phase offset value in the master device to produce a stored offset value and a stored control offset value, respectively; and

using the stored offset value in the transmission of data from the master device to the first slave device over the data line and using the stored control offset value in the transmission of control information from the master device to the second slave device over the request line.

32. (Previously Presented) The method of claim 31, wherein using the stored control offset value further comprises:

adjusting the phase of a clock signal based on the stored control offset value to produce a phase adjusted clock signal; and

transmitting control information over the request line based on the phase adjusted clock signal.

33. (Previously Presented) The method of claim 32, wherein transmitting control information over the request line further comprises driving the control information on the request line using an output buffer, wherein the timing of the output buffer is controlled based on the phase adjusted clock signal.

34. (Previously Presented) The method of claim 31, wherein the control information includes a slave access request.

35. (Previously Presented) The method of claim 21, wherein using the stored offset value further comprises using the stored offset value in the transmission of data over a plurality of data lines.

36. (Previously Presented) The method of claim 35, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

driving data on the plurality of data lines using a corresponding plurality of output buffers, wherein timing of each output buffer of the plurality of output buffers is controlled based on the stored offset value.

37. (Currently Amended) A method for calibrating transmission of ~~control~~ information from a master device to a ~~first~~ slave device ~~over a request line~~, comprising:

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~~determining a phase offset value corresponding to control information transmission from the master device to the first slave device over the request line;~~

determining a plurality of phase offset values for synchronizing communication between a master device and a slave device;

storing the phase offset values in an addressable phase value register bank ~~in the master device to produce a stored offset values~~;

retrieving ~~the~~ a stored offset value from the addressable phase value register bank; and

using the stored offset value in the transmission of ~~control~~ information from the master device to the ~~first~~ slave device ~~over the request line~~.

38. (Currently Amended) The method of claim 37, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

transmitting control information over ~~the~~ a request line based on the phase adjusted clock signal.

39. (Currently Amended) The method of claim 38, wherein transmitting control information over the request line further comprises driving the control information on ~~the~~ a data line using an output buffer, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

40. (Currently Amended) The method of claim 37, wherein determining the phase offset value further comprises sending data to the ~~first~~ slave device.

41. (Currently Amended) The method of claim 40, wherein sending data to the ~~first~~ slave device further comprises sending data to the ~~first~~ slave device over the request line.

42. (Currently Amended) The method of claim 40, wherein determining the phase offset value further comprises receiving the data sent to the ~~first~~ slave device, from the ~~first~~ slave device.

43. (Currently Amended) The method of claim 42, wherein determining the phase offset value further comprises comparing phase of the data received from the ~~first~~ slave device with phase of a clock signal.

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44. (Currently Amended) The method of claim 43, wherein the data is sent to the ~~first~~ slave device over the request line, and wherein the data is received from the ~~first~~ slave device over a data line.

45. (Previously Presented) The method of claim 37, wherein the phase offset value is stored with a plurality of additional phase offset values in the master device.

46. (Previously Presented) The method of claim 37, wherein the phase offset value is adjusted by a margin offset.

47. (Previously Presented) The method of claim 37, wherein using the stored offset value further comprises using the stored offset value in the transmission of control information over a plurality of request lines.

48. (Previously Presented) The method of claim 47, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

driving control information on the plurality of request lines using a corresponding plurality of output buffers, wherein timing of each output buffer of the plurality of output buffers is controlled based on the stored offset value.

49. (Currently Amended) The method of claim 37, wherein the ~~control~~ information transmitted to the slave device is a portion of an access request.

50. (Previously Presented) A master device operable to transmit data to a first slave device over a data line, the master device comprising:

a phase aligner operable to determine a phase offset value corresponding to data transmission from the master device to the first slave device over the data line, wherein the phase aligner includes an addressable phase value register bank operable to store the phase offset value as a stored offset; and

an output buffer operably coupled to the phase aligner, wherein the output buffer is operable to drive the data on the data line based on the stored offset in a first register of the addressable phase value register bank.

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51. (Previously Presented) The master device of claim 50, wherein the phase aligner includes a phase rotator operable to receive a clock signal, wherein the phase rotator is operable to generate a phase adjusted clock signal from the clock signal based on the stored offset, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

52. (Previously Presented) The master device of claim 51, wherein the phase rotator includes a phase locked loop.

53. (Previously Presented) The master device of claim 51, wherein the phase rotator includes a delay locked loop.

54. (Previously Presented) The master device of claim 50, wherein the phase aligner periodically determines the phase offset value corresponding to data transmission and stores the periodically determined phase offset value in the first register.

55. (Previously Presented) The master device of claim 50, wherein the phase offset value is at least partially based on flight time of the data on the data line.

56. (Previously Presented) The master device of claim 50 further comprising a logic block operable to generate data that is sent to the first slave device in order to determine the phase offset value.

57. (Previously Presented) The master device of claim 50 further comprising receiving circuitry operable to receive data from the first slave device, wherein the data received from the first slave device is used by the phase aligner to determine the phase offset value.

58. (Previously Presented) The master device of claim 57, wherein the phase aligner is operable to compare the data received from the first slave device with a clock signal to determine the phase offset value.

59. (Previously Presented) The master device of claim 50 further comprising a plurality of output drivers coupled to the phase aligner, wherein each output driver of the plurality of output drivers drives data onto a corresponding data line based on the stored offset.

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60. (Previously Presented) A master device operable to transmit data to a first slave device over a data line and control information to a second slave device over a request line, the master device comprising:

a phase aligner operable to determine a phase offset value corresponding to data transmission from the master device to the first slave device over the data line and a control phase offset value corresponding to control information transmission from the master device to the second slave device over the request line, wherein the phase aligner includes a first register operable to store the phase offset value as a stored offset and a second register operable to store the control phase offset value as a stored control phase offset;

a first output buffer operably coupled to the phase aligner, wherein the first output buffer is operable to drive the data on the data line based on the stored offset; and

a second output buffer operably coupled to the phase aligner, wherein the second output buffer is operable to drive the control information on the request line based on the stored control phase offset.

61. (Previously Presented) The master device of claim 60 further comprising a control output driver operably coupled to the phase aligner, wherein the control output driver is operable to drive control information on the request line based on the stored control offset.

62. (Previously Presented) The master device of claim 61, wherein the phase aligner includes a phase rotator operable to receive a clock signal, wherein the phase rotator is operable to generate a phase adjusted clock signal from the clock signal based on the control phase offset, wherein timing of the control output driver is controlled based on the phase adjusted clock signal.

63. (Previously Presented) The master device of claim 60 further comprising a plurality of control output drivers operably coupled to the phase aligner, wherein each control output driver of the plurality of control output drivers is operable to drive control information on a corresponding request line based on the stored control offset.

64. (Previously Presented) A master device operable to transmit control information to a first slave device over a request line, the master device comprising:

a phase aligner operable to determine a phase offset value corresponding to control information transmission from the master device to the first slave device over the request line, wherein the phase aligner includes an addressable phase value register bank operable to store the phase offset value as a stored offset; and

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an output buffer operably coupled to the phase aligner, wherein the output buffer is operable to drive the control information on the request line based on the stored offset in a first register of the addressable phase value register bank.

65. (Previously Presented) The master device of claim 64, wherein the phase aligner includes a phase rotator operable to receive a clock signal, wherein the phase aligner is operable to generate a phase adjusted clock signal from the clock signal based on the stored offset, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

66. (Previously Presented) The master device of claim 65, wherein the phase rotator includes a phase locked loop.

67. (Previously Presented) The master device of claim 65, wherein the phase rotator includes a delay locked loop.

68. (Previously Presented) The master device of claim 64, wherein the phase aligner periodically determines the phase offset value corresponding to data transmission and stores the periodically determined phase offset value in the first register.

69. (Previously Presented) The master device of claim 64, wherein the phase offset value is at least partially based on flight time of the control information on the request line.

70. (Previously Presented) The master device of claim 74 further comprising a logic block operable to generate data that is sent to the first slave device in order to determine the phase offset value.

71. (Previously Presented) The master device of claim 64 further comprising receiving circuitry operable to receive data from the first slave device, wherein the data received from the first slave device is used by the phase aligner to determine the phase offset value.

72. (Previously Presented) The master device of claim 71, wherein the phase aligner is operable to compare the data received from the first slave device with a clock signal to determine the phase offset value.

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73. (Previously Presented) The master device of claim 64 further comprising a plurality of output drivers coupled to the phase aligner, wherein each output driver of the plurality of output drivers outputs drives control information onto a corresponding request line based on the stored offset.

74. (New) A method of operating a master/slave system, said method comprising the steps of:

assessing a plurality of phase delays required for synchronized communication between a master device and a plurality of slave devices over a shared communication channel;

identifying a selected phase delay from said plurality of phase delays for a selected slave device of said plurality of slave devices; and

communicating information over said shared communication channel between said master device and said selected slave device of said plurality of slave devices in accordance with said selected phase delay.

75. (New) A master/slave system, comprising:

a plurality of slave devices, each slave device including a clock circuit without phase alignment circuitry; and

a master device with a universal phase alignment circuit including an addressable phase value register bank storing a plurality of phase values for said plurality of slave devices, said master device utilizing a selected phase value of said plurality of phase values to alter a system clock signal in accordance with said selected phase value so as to establish synchronous communication between said master device and a selected slave device of said plurality of slave devices over a shared communication channel coupling said master device to each of said plurality of slave devices.

C1 Concl